Listing and Amendments to the Claims

This listing of claims will replace the claims that were published as annexes to the International Preliminary Examination Report:

1. (currently amended) Method for setting an operating parameter in a peripheral IC ~~(12)~~ of an electronic appliance, in which method the operating parameter is transmitted from a central IC ~~(15)~~ in the electronic appliance via a bus connection ~~(19)~~ to the peripheral IC ~~(12), characterized in that~~ wherein the operating parameter is buffered in a preregister ~~(24)~~ of the peripheral IC ~~(12)~~ while a working process is running with the current operating parameter stored in a working register ~~(25)~~ and that the buffered operating parameter is transferred to said working register ~~(25)~~ to become active in the working process only if a transfer signal has been sent from the central IC ~~(12)~~ via the bus connection ~~(19)~~.

2. (currently amended) Method as claimed in Claim 1, in which method the bus connection ~~(19)~~ is a serial bus connection with a data line ~~(Data)~~, a control line ~~(Start)~~ and a clock line ~~(CLK)~~, and the transfer signal is transmitted via the control line ~~(Start)~~ to the peripheral IC ~~(12)~~.

3. (currently amended) Method as claimed in Claim 1 ~~or 2~~, in which method the start of a data transmission from the central IC ~~(15)~~ to the peripheral IC is also signaled via the control line ~~(Start)~~.

4. (currently amended) Method according to claim 2 ~~or 3~~, in which the register write address for writing to the preregister ~~(24)~~ is transferred to the peripheral IC ~~(12)~~ on the data line ~~(Data)~~ ahead of the operating parameter.

5. (currently amended) Method according to ~~one of claims 2 to 4~~ claim 2, in which the start signal occurs on the control line ~~(Start)~~ with a rising or falling edge of a clock signal on the clock line ~~(CLK)~~ and the transfer signal occurs on the control line ~~(Start)~~ with a falling or rising edge of a clock signal on the clock line ~~(CLK)~~.

6. (currently amended) Device for carrying out the method as claimed in ~~one of the preceding claims~~ claim 1 with a central IC ~~(15)~~ and a peripheral IC ~~(12)~~, with a bus connection ~~(19)~~ between the central IC ~~(15)~~ and the peripheral IC ~~(12)~~, where the peripheral IC ~~(12)~~ has a working register ~~(25)~~ for an operating parameter, ~~characterized in that~~ wherein the peripheral IC ~~(12)~~ also has a preregister ~~(24)~~ for buffering an operating parameter while a working process is running with the current operating parameter stored in a working register ~~(25)~~, said operating parameter is received via the bus connection ~~(19)~~, and wherein the device has means for transferring the buffered value to the working register ~~(25)~~ to become active in the working process, which means respond to a transfer signal that is transmitted from the central IC ~~(15)~~ via the bus connection ~~(19)~~.

7. (currently amended) Device as claimed in Claim 6, in which device the bus connection ~~(19)~~ is a serial bus connection with a data line ~~(Data)~~, a control line ~~(Start)~~ and a clock line ~~(CLK)~~, and the control line ~~(Start)~~ is used to transmit the transfer signal.

8. (currently amended) The device as claimed in Claim 7, in which device the control line ~~(Start)~~ is also used to transmit a start signal for data transmission from the central IC ~~(15)~~ to the peripheral IC ~~(12)~~.

9. (currently amended) Device according to claims 7 ~~or 8~~, including bus protocol means according to which the register write address for writing to the preregister ~~(24)~~ is transferred to the peripheral IC ~~(12)~~ on the data line ~~(Data)~~ ahead of the operating parameter.

10. (currently amended) Device according to ~~one of claims 7 to 9~~ claim 7, including signaling means according to which the start signal occurs on the control line ~~(Start)~~ with a rising or falling edge of a clock signal on the clock line ~~(CLK)~~ and the transfer signal occurs on the control line ~~(Start)~~ with a falling or rising edge of a clock signal on the clock line ~~(CLK)~~.

11. (currently amended) Device according to ~~one of the claims 6 to 10~~ claim 6, in which device the peripheral IC ~~(12)~~ relates to a front-end IC for a communication arrangement for wireless data transmission and the central IC ~~(15)~~ relates to a signal processing device, with means for modulation or demodulation of the mixed RF input signal and for further signal processing in baseband.

12. (currently amended) Device as claimed in Claim 11, in which device the operating parameter relates to the gain setting for the receive gain in the front-end IC ~~(12)~~.

13. (currently amended) Device according to ~~one of the claims 6 to 12~~ claim 6, which device is configured as a send and receive device for wireless data transmission in accordance with the HIPERLAN2 standard.